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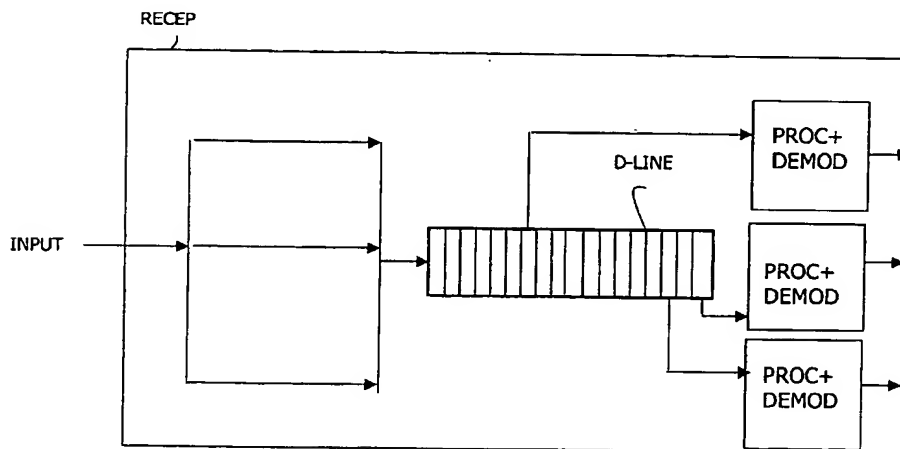
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(54) Title: **DELAY LINE FOR MULTIPLE PROPAGATION PATHS RECEPTION**



(57) Abstract: The present invention relates to a delay line (D LINE) for delaying an input signal, said input signal comprising a series of samples (IN TIME, LATE, VOID). The invention is characterized in that it is intended to delay the input signal by a series of delays and that the series is divided into a series of delay sub-lines (ZONE) each intended to write one sample from the series of samples (IN TIME, EARLY, LATE, VOID) of said input signal, and in that it comprises control means (RD DD GEN) intended to generate read addresses of the samples in the delay sub-line (ZONE) from the series of samples (IN TIME, EARLY, LATE, VOID) of the input signal. The read addresses are equal to a difference between a write address of a sample in the delay sub-lines (ZONE) of the input signal and said delays expressed in a number of chip periods.

WO 2004/019510 A1